

Software configures IBM PC interrupts

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Anyone who has installed an expansion card in an IBM PC-AT expansion slot has dealt with interrupt conflicts. Often, despite the manufacturer's claims of "plug-and-play" compatibility, inserting a simple I/O card turns a fully functional computer into a brain-dead piece of equipment. Interrupt assignments and the possible resulting conflicts usually cause this pernicious problem.

Under software control, the circuit in Fig 1 can dynamically assign an interrupt-channel to an I/O card based on available channels. (The new PCI bus from Intel uses the same methodology.)

The 8-bit ISA bus provides six external-interrupt lines for expansion cards. Because the assignment of these interrupts is not standardized, more than one card may come from its factory set to the same interrupt line.

Now, multiple cards that use the same interrupt line are not necessarily bad. The ISA bus permits multiple cards assigned to the same interrupt. In fact, serial-I/O cards frequently use this scheme because PCs come hardwired with

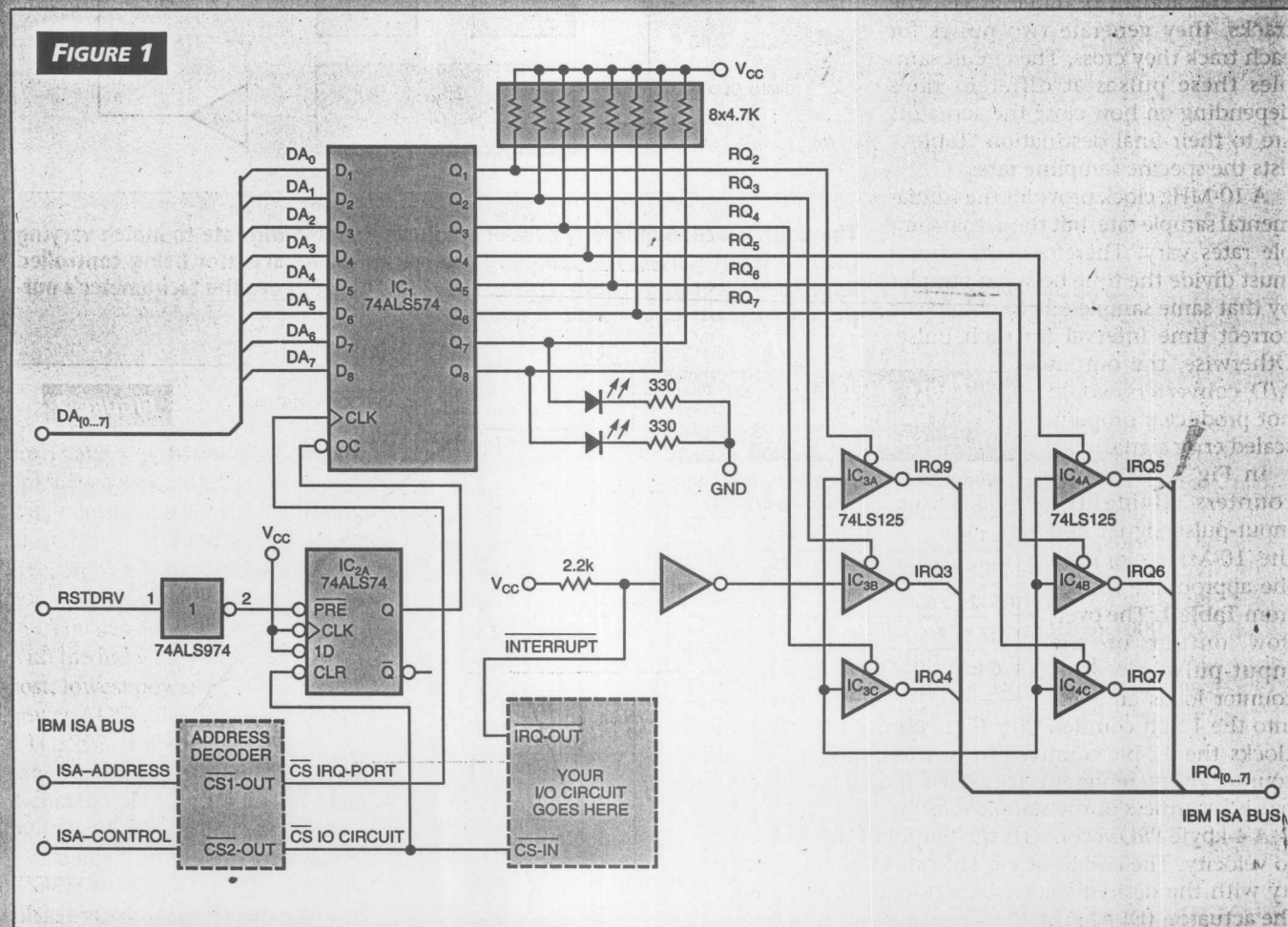
COM1 sharing an interrupt line with COM3 and COM2 with COM4.

But, in some cases, the interrupt-handler software cannot resolve such a conflict and the system crashes. Instead of forcing the user to troubleshoot the system by tediously changing jumper settings, the circuit allows the software to reconfigure the I/O board. Today's users demand such comfort and find any other setup highly anachronistic.

The heart of the circuit is an 8-bit register, IC₁, that stores the selected interrupt for the card. The software selects an interrupt line by writing a zero into the corresponding register bit. The software must first set all unselected interrupt bits to a logic 1. You can use the two leftover most-significant bits as general-purpose output bits. In our case, we used the bits to drive two status LEDs.

Your main concern is the circuit's cold-start behavior. The circuit must deactivate all interrupts upon power-up because the status of the register is undefined. The PC's reset-driver signal presets flip-flop IC_{2A} at power-up and disables IC₁'s out-

FIGURE 1



A simple setup program can dynamically assign an interrupt-channel to an IBM PC's I/O card, based on currently available channels.

puts. The resistor pullups ensure that the tri-state interrupt line-drivers of IC₃ and IC₄ are inactive and can't assert any interrupts.

At this time, the interrupt driver can find a free interrupt line by checking the CPU's interrupt-vector table. After finding an unused interrupt, the software activates the add-in board's interrupt line by writing a logic 0 into its register. The system is active but not triggered.

The software initializes the board's I/O-port controller. The first chip-select of the I/O controller resets flip-flop IC_{2A}.

In turn, this action activates the output of the interrupt register IC₁. Now the controller's interrupt requests can propagate through the 74LS125 drivers to the CPU. Pushing reset deselects all interrupts on the board, and the system is clean again.

This circuit works in both 8- and 16-bit IBM expansion slots. To use all available interrupts you need an IBM-AT, a second register, and some more 74LS125 drivers. (DI #1614)

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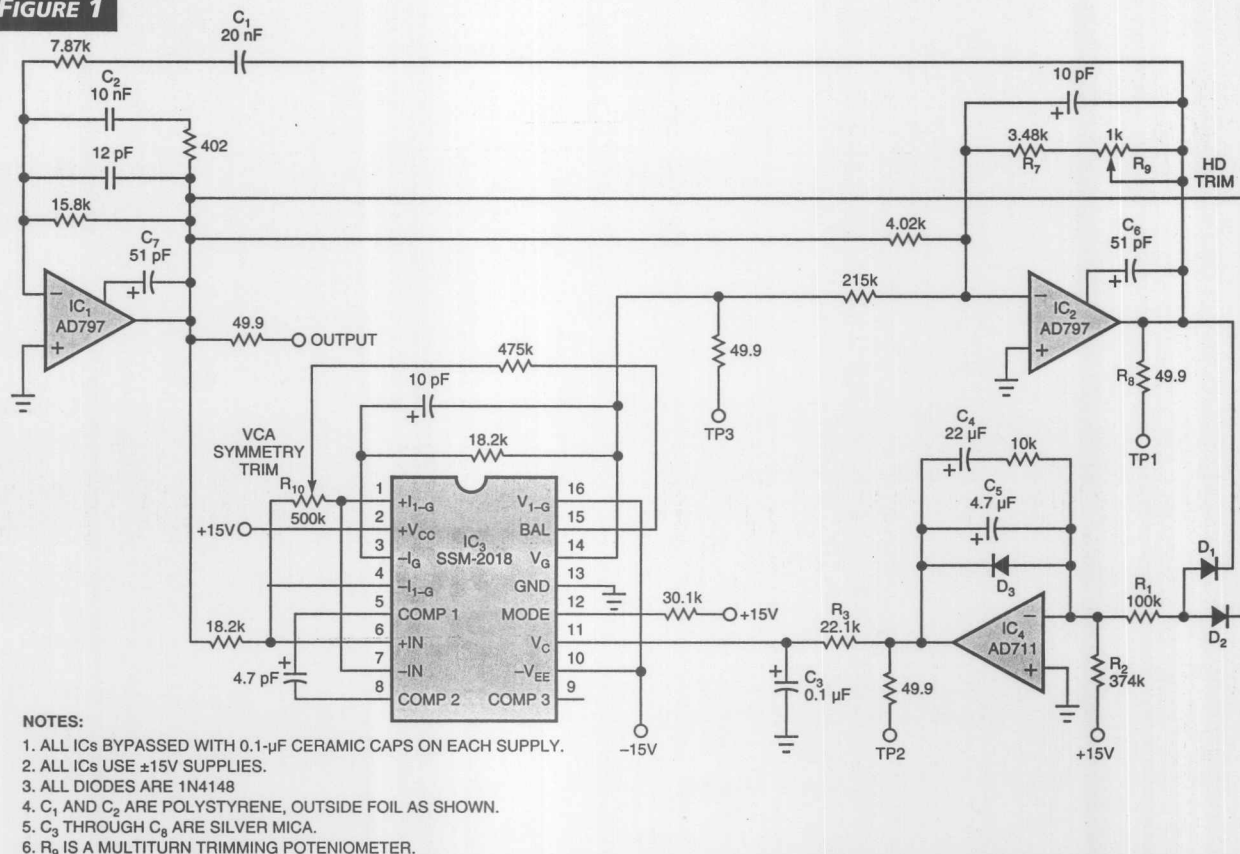
The Wien-bridge sine-wave oscillator uses a light bulb to stabilize its amplitude. The circuit in Fig 1 doesn't have a light bulb; it sports several enhancements that lower its distortion and generate a test signal pure enough for testing modern op amps and high-resolution A/D converters.

IC₁ and associated components form the Wien-bridge and function as a bandpass filter. IC₁'s output goes to the voltage-

controlled amplifier (VCA), IC₃. IC₃ acts as a "smart resistor" whose value the circuit continuously adjusts via IC₄. IC₂ adds the outputs of IC₁ and the VCA and feeds the result into the bridge. These two op-amp inverters eliminate any common-mode signal that might limit performance.

The circuit's AGC loop begins with diodes D₁ and D₂. These diodes half-wave rectify the outputs of IC₁ and IC₂.

FIGURE 1



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